ANALOG DEVICES

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AN-279
APPLICATION NOTE

Using the AD650 Voltage-to-Frequency Converter As a Frequency-to-Voltage Converter

By Steve Martin

The AD650 is a versatile monolithic voltage-to-frequency converter (VFC) that utilizes a charge balanced architecture to obtain high performance in many applications. Like other charge balanced VFCs the AD650 can be used in a reverse mode as a frequency-to-voltage (F/V) converter. This application note discusses the F/V architecture and operation, component selection, a design example, and the fundamental trade-off between output ripple and circuit response time.

F/V CIRCUIT ARCHITECTURE

Figure 1 shows the major components of the frequency-to-voltage (F/V) converter. It includes a comparator, a one-shot with a switch, a constant current source, and a lossy integrator. When the input signal crosses the threshold at the comparator input, the comparator triggers the one-shot. The one-shot controls a single pole double throw switch which directs the current source to either the summing junction, or the output, of the lossy integrator. When the one-shot is in its "on" state, there is current injected into the input of the integrator and its output rises. When the one-shot period has passed, the current is steered to the output of the integrator. Since the output is a low impedance node, the current has no effect on the circuit and is effectively turned off. During this time the output falls due to the discharge of C_{INT} through R_{INT}. When there is constant triggering applied to the comparator, the integration capacitor will charge to a relatively steady value and be maintained by constant charging and discharging. The charge stored on C_{INT} is unaffected by loading because of the low output impedance of the op amp.

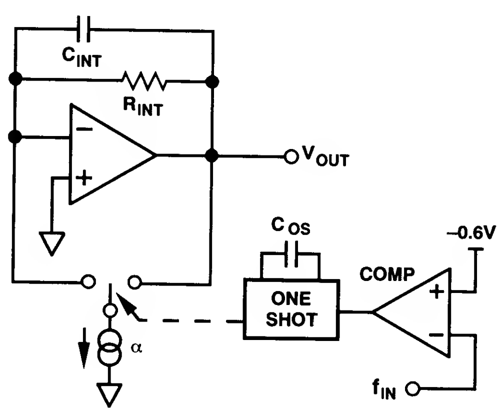

Figure 1. Circuit Architecture

THEORY OF OPERATION

Figure 2 shows a simplified representation of the AD650 in the F/V mode. Figure 3 represents the current i(t) delivered to the lossy integrator. The current can be thought of as a series of charge packets delivered at frequency $f_{IN} = \frac{1}{T}$ with constant amplitude (α) and duration (t_{OS}).

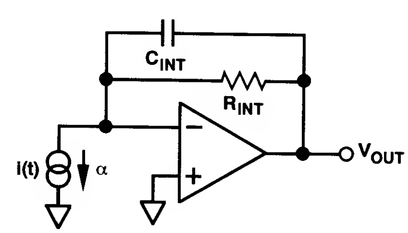

Figure 2. Simplified Schematic

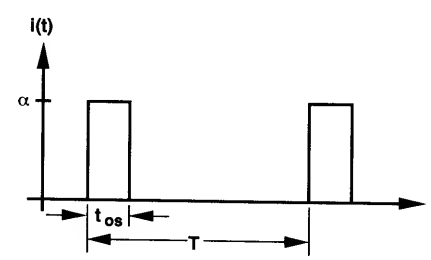

Figure 3. Current i(t) into Integrator

From inspection of Figure 3 the average value of input current is found by dividing the area of the current i(t) by the period T. The dc component of the output voltage is found by scaling the average input current by the feedback resistor R_{INT}.

$$V_{OUTAVG} = \frac{\alpha\, t_{OS}}{T} \cdot R_{INT} \qquad (1a)$$

Equation 1a becomes a linear function of frequency when f_{IN} is substituted for $\frac{1}{T}$.

$$V_{OUTAVG} = t_{OS} \cdot R_{INT} \cdot \alpha \cdot f_{IN} \qquad (1b)$$

Notice that the relationship between the average output voltage and input frequency is a function of the one-shot time constant and the feedback resistor but not of the integration capacitor. This is because the integration capacitor is an open circuit to dc. From Equation 1b it's clear that the most practical way to trim the full-scale voltage is to include a trim potentiometer in series with R_{INT}. Typically a 30% trim range will be required to absorb errors associated with t_{OS} and α.

It is also important to characterize the transient response of the integrator in order to determine settling time of the F/V to a step change of input frequency. The transfer function of the lossy integrator is given in the frequency domain by:

$$\frac{V_{OUT}(S)}{I_{IN}(S)} = \frac{\frac{1}{C_{INT}}}{S + \frac{1}{R_{INT} \cdot C_{INT}}} \qquad (2)$$

which indicates that the natural or step response to a change of input frequency is governed by an exponential function with time constant $\tau = R_{INT} \cdot C_{INT}$.

With the average output voltage and transient response known, the peak-peak output ripple can be determined using Equation 3. Once this is determined, a design algorithm can be developed. The derivation of Equation 3 is provided in Appendix A.[1]

The peak-peak ripple is given by:

$$V_{PP} = \frac{e^{t_{OS}/RC} - e^{T/RC} + e^{(T-t_{OS})/RC} - 1}{1 - e^{T/RC}} \cdot \alpha \cdot R \qquad (3)$$

where:

t_{OS}	= one-shot time constant	[seconds]
T	= period of input frequency ($1/f_{IN}$)	[hertz]
R	= integration resistor	[ohms]
C	= integration capacitor	[farads]
α	= current source value (1mA for AD650)	[amps]

Equation 3 accurately represents the ripple amplitude for a given design. The following section shows how this equation is used as an iterative part of the total solution. Equation 3 can also be used to illustrate how the ripple amplitude changes as a function of input frequency. It is interesting to note that the ripple amplitude changes only moderately with input frequency and has its largest magnitude at the minimum frequency.

DESIGN PROCEDURE

Recall from looking at Figure 3, the one-shot "on" time will be some fraction of the total input period. This is the time that the circuit integrates the current signal α. The output ripple can be minimized by allowing the current source to be on during the majority of this period. This is achieved by choosing the one-shot time constant so that it occupies almost the full period of the input signal when this period is at its minimum (or the input frequency at its maximum). To design safely and allow for component tolerance at f_{max}, make t_{OS} approximately equal to 90% of the minimum period. Given t_{OS}, the value of the one-shot timing capacitor, C_{OS}, is determined from Equation 1 in the AD650 data sheet. This equation has been rearranged and appears here as:

$$C_{OS} = \frac{t_{OS} - 3 \cdot 10^{-7}\, sec}{6.8 \cdot 10^{3}\, sec/F} \qquad (4)$$

[NOTE: For maximum linearity performance use a low dielectric absorption capacitor for C_{OS}.]

where t_{OS} is in seconds and C_{OS} is in farads.

Once C_{OS} is known, the integration resistor is uniquely determined from the full-scale equation (Equation 1b), since t_{OS}, α, f_{IN}, and V_{OUT} are known. This leaves only the integration capacitor as the final unknown.

C_{INT} is chosen by first determining the response time of the device being measured. If, for example the frequency signal to be measured is derived from a mechanical device such as an aircraft turbine shaft, the momentum of the shaft and the blades should be used to determine the response time. The time constant of the F/V is then set to match the time constant of the mechanical system. It may be set somewhat lower depending on the desired total response time of the mechanical and electrical system. Remember to allow several time constants (N) for the F/V to approach its final value. For the first iteration of C_{INT} use the following expression:

$$C_{INT} = \frac{\text{Mechanical Response Time}}{N \cdot R_{INT}} \qquad (5)$$

where N is the number of time constants chosen to allow adequate settling. Table I may be used to determine the number of time constants required for given settling accuracy.

Table I. Settling Accuracy vs. Number of Time Constants

# of Time Constants (N)	# of Bits	% Accuracy
4.16	6	1.6
4.85	7	0.8
5.55	8	0.4
6.23	9	0.2
6.93	10	0.1
7.62	11	0.05
8.30	12	0.024
9.00	13	0.012
9.70	14	0.006
10.4	15	0.003
11.0	16	0.0015

[1]The essence of the solution was captured by McGillem and Cooper in [1].

A larger number of time constants will give a more responsive circuit but will also increase the ripple at the F/V output. A practical approach is to start with 8 bit settling accuracy using N = 6 time constants and increase or decrease N depending on ripple content.

The ripple content is calculated using Equation 3. Remember that the ripple amplitude will change with frequency and will be largest at the lowest frequency. It is also important to note that while in some cases the ripple amplitude may be large, the *average* value of the output voltage will always represent the input frequency (unless the ripple gets too close and "clips" at the positive supply rail). Figure 4 shows an example of how output ripple amplitude will change with input frequency for a typical application. This graph was obtained by plotting Equation 3 over the full range of input

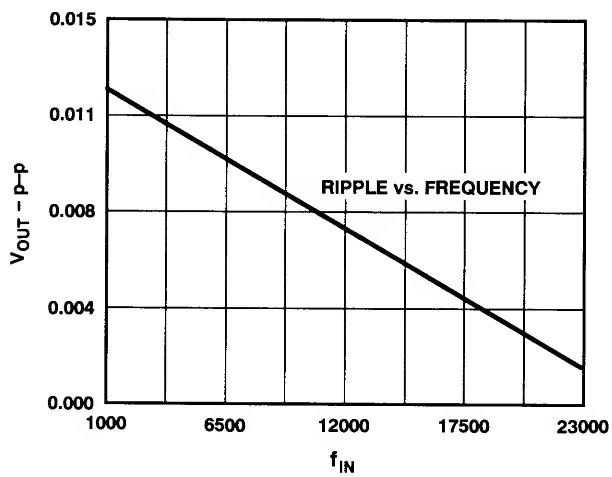

Figure 4. P-P Ripple vs. Frequency (See Design Example)

frequencies. For design purposes it is only necessary to calculate ripple at the worst case frequency (f_{min}). Figure 5 summarizes the design procedure.

DESIGN EXAMPLE

The rpm of an automobiles engine is to be monitored for use by an on-board computer. The rpm signal which will be generated from an F/V converter is to be digitized with an 8-bit A/D converter. The rpm range of the engine extends from 300 rpm to 7000 rpm. A 200 tooth flywheel at these rotational speeds will generate pulses from 1 kHz up to 23 kHz. The response time to a step change in throttle position of the engine has been measured, in neutral, to be 400 ms. The goal is to design an F/V converter that will respond at approximately the same rate as the engine or faster and will have ripple that is undetectable by the A/D converter. The A/D converter has a ten volt full scale.

1. Let t_{OS} be $0.9 \cdot \frac{1}{f_{max}} = 0.9 \times 43.5\ \mu s = \mathbf{39\ \mu s}$.
2. Find C_{OS} = **0.0057** μF (from Equation 4) (an impractical value for polystyrene, but tantalum may be used with reduced linearity).
3. $R_{INT} = \frac{10\ V}{1\ mA \cdot 39\ \mu s \cdot 23\ kHz} = \mathbf{11.14\ k\Omega}$ (from Equation 1b).

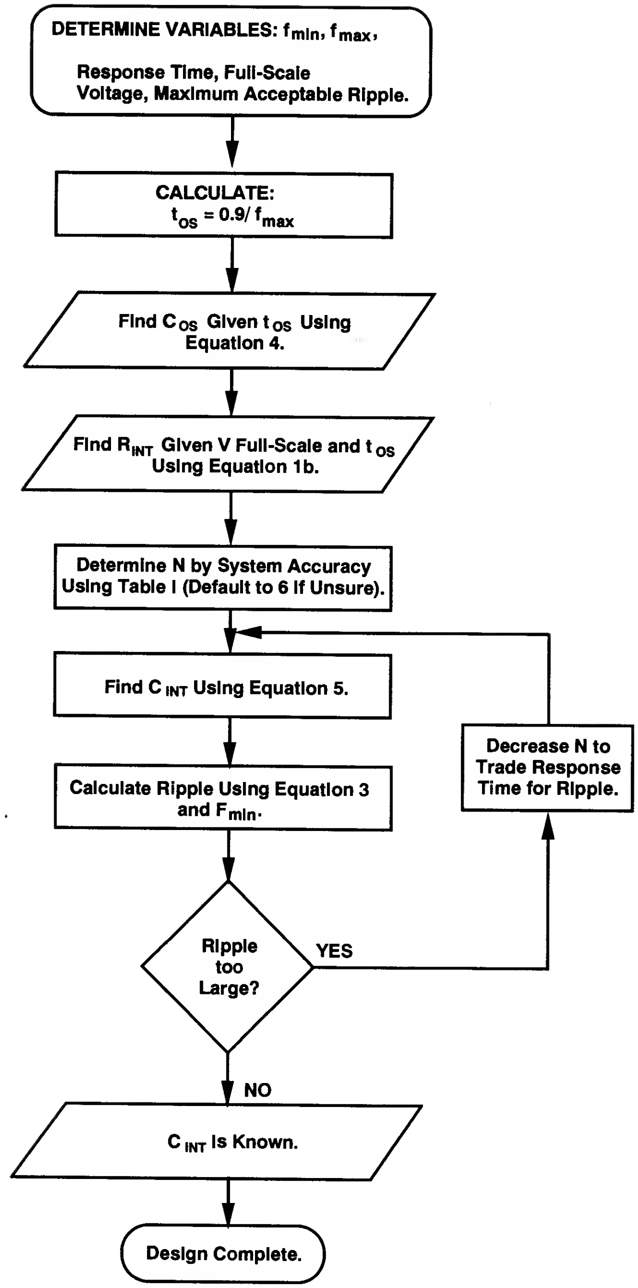

Figure 5. Design Flowchart

(If R_{INT}, the load seen by the amplifier, is less than 1 kΩ, then t_{OS} must be reevaluated.)

4. From Table I an RC network can settle to 8 bits in 6 time constants so: $C_{INT} = \frac{400\ ms}{(6)\ 11.14\ k\Omega} = \mathbf{6\ \mu F}$.
5. Ripple = 6.25 mV @ 300 rpm and 0.67 mV @ 7000 rpm (from Equation 3).
6. 1/2 LSB size for an 8-bit converter with 10 V full scale is 19.5 mV. Fortunately the ripple is below the quantization level on the first iteration. If desired, the integration capacitor may be lowered to reduce response time of the F/V converter.
7. Guessing C_{INT} = 3.0 μF or using an iterative computer program gives a maximum ripple content of 12.5 mV and a response time of 200 ms.

THE TRADE-OFF BETWEEN RIPPLE AND RESPONSE TIME

In many instances some compromise must be made between ripple and response time. If response time is of primary importance, the integration capacitor may be lowered at the expense of increased ripple. Similarly, if ripple is paramount, the integration capacitor must be increased resulting in slower response. The design procedure outlined above assumes that ripple content is the less desirable effect. Rather than increasing C_{INT}, a low-pass filter could be used, but this also slows the response time. An approximation to determine total response time of two cascaded systems, each with separate response times, can be found by using the "root sum of squares" technique.

$$T_{TOTAL} = \sqrt{T_A^2 + T_B^2}$$

This leads to the "three to one" rule, i.e., if T_A is more than three times T_B and their squares are added, T_B may be ignored, hence, T_A is the total response time of the system.

SUMMARY

Low cost voltage-to-frequency converters can be used in the frequency-to-voltage mode. Trade-offs exist between output settling time and ripple with the selection being application specific. However using the design guidelines highlighted in this note, optimized performance can be achieved in many applications.

References

[1] McGillem, C. D., and G. R. Cooper, *Continuous and Discrete Signal and System Analysis,* Second Edition. New York: CBS College Publishing, 1984.

[2] Analog Devices Inc. *AD650 Data Sheet*
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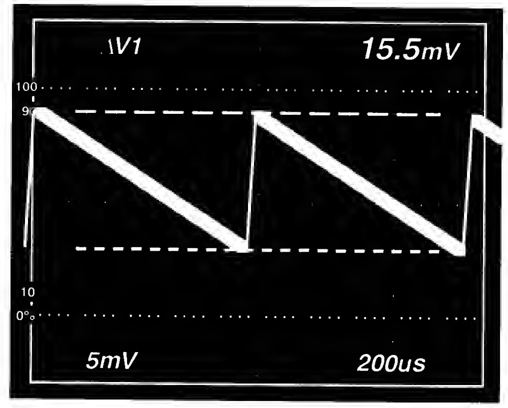

Figure 6. Typical Ripple Output

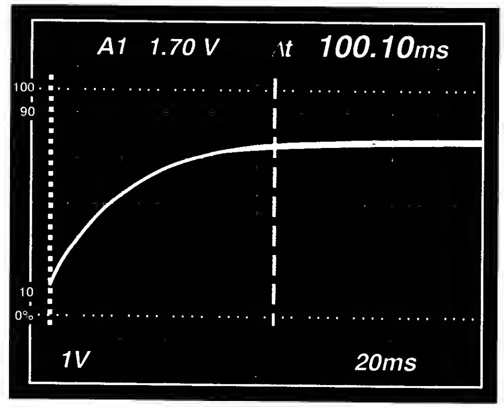

Figure 7. Response to Step Change in Frequency

NOTE

This circuit of Figure 8 should be used in place of the one shown in Figure 6 of the AD650 data sheet if the input signal has slower edges than the one-shot time delay. In such cases the comparator has a tendency to "double trip" possibly giving inaccurate results. This new circuit uses the open collector output to pull down on the input signal until the one-shot period occurs. After this time it gets pulled up by the +5 V supply. This circuit may not be needed for all applications since fast edges such as a TTL signal will give accurate results with the previous configuration. This circuit has the disadvantage of requiring a +5 V supply and increased power consumption.

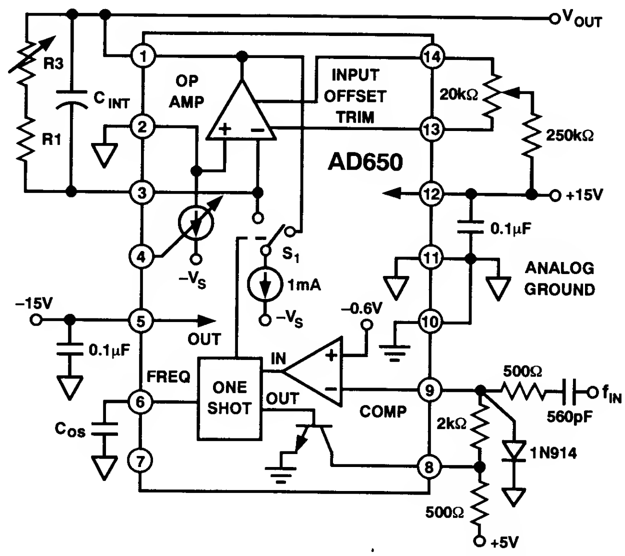

Figure 8. Circuit Showing Modified Input Structure

APPENDIX A: DERIVATION OF RIPPLE EQUATION

From Figure 2, one period I(t) is given by:

$$I_T(t) = \alpha[u(t) - u(t-t_{OS})] \text{ where } \alpha = 1\ mA$$

$$L\{I_T(t)\} = \alpha\left[\frac{1}{S} - \frac{1}{S}e^{-St_{os}}\right] = \frac{\alpha}{S}(1 - e^{-St_{os}})$$

Using the rule for repeated cycles gives:

$$I_P(S) = I_T(S)\frac{1}{1 - e^{-TS}} \text{ so } I_P(S) = I(S) = \frac{\alpha}{S}\frac{[1 - e^{-St_{os}}]}{[1 - e^{-TS}]}$$

From Figure 2 we have:

$$i(t) = \frac{V_{OUT}(t)}{R} + C\frac{dV_{OUT}(t)}{dt} \text{ which gives:}$$

$$I(s) = V_{OUT}(S)\left[\frac{1}{R} + SC\right]$$

$$\text{so } \frac{V_{OUT}(S)}{I(S)} = \frac{\frac{1}{C}}{\left[S + \frac{1}{RC}\right]}$$

but using I(S) from above gives:

$$V_{OUT}(S) = V_{TOTAL}(S) = \frac{1}{S}\frac{\frac{\alpha}{C}}{\left(S + \frac{1}{RC}\right)}\frac{[1 - e^{-St_{os}}]}{[1 - e^{-TS}]}$$

The transient portion of the solution results from evaluating this expression at the frequency $S = -\frac{1}{RC}$ which gives the residue:

$$V_{TRANS}(S) = \frac{1}{\left(-\frac{1}{RC}\right)}\frac{[1 - e^{t_{os}/RC}]}{[1 - e^{T/RC}]}\frac{\alpha}{C}\frac{1}{\left(S + \frac{1}{RC}\right)}$$

which can be called $\frac{\beta}{S + \frac{1}{RC}}$ for simplicity

$$\text{where } \beta = \frac{\alpha}{\left(-\frac{1}{R}\right)}\frac{[1 - e^{t_{os}/RC}]}{[1 - e^{T/RC}]}$$

and so $V_{TRAN}(t) = \beta e^{-t/RC}\,u(t)$

The total response of the system is the sum of the transient response and the steady state response:

or $V_{TOTAL}(S) = V_{TRAN}(S) + V_{SS}(S)$ and so:

$V_{SS}(S) = V_{TOTAL}(S) - V_{TRAN}(S)$

using V_{TOTAL} and V_{TRAN} from above gives:

$$V_{SS}(S) = \frac{\alpha}{CS}\frac{[1 - e^{-St_{os}}]}{\left(S + \frac{1}{RC}\right)[1 - e^{-TS}]} - \frac{\beta}{S + \frac{1}{RC}}$$

which can be massaged into $\dfrac{\frac{\alpha}{C} - \frac{\alpha}{C}e^{-St_{os}} - \beta S + \beta s e^{TS}}{S\left(S + \frac{1}{RC}\right)(1 - e^{TS})}$

If we are interested in just one period of the steady state solution we can drop all periods but the first by simply removing all terms containing e^{TS} (again this goes back to the rule for laplace transform of a periodic function given just one period),

$$\text{so: } V_{SS}(t) = \frac{\frac{\alpha}{C} - \frac{\alpha}{C}e^{-Stos} - \beta S}{s\left(S + \frac{1}{RC}\right)}$$

and for the solution as it exists before t_{OS} drop all e^{-Stos} terms

$$\text{leaving: } \frac{\frac{\alpha}{C} - \beta S}{S\left(S + \frac{1}{RC}\right)}$$

which can be represented as:

$\dfrac{\alpha R}{S} - \dfrac{\alpha R + \beta}{\left(S + \frac{1}{RC}\right)}$ by using partial fraction expansion.

So now $V_{SS}(t) = [\alpha R - (\alpha R + \beta)e^{-t/RC}]\,u(t)$ for $0 < t < t_{OS}$. $V_{SS}(t)$ for the second half of the period ($t_{OS} < t < T$) can be found by subtracting all terms containing e^{-Stos} from the solution before t_{OS}.

$$V_{SS}(t) = [\alpha R - (\alpha R + \beta)\,e^{-t/RC}]\,u(t) - L^{-1}\left\{\frac{\frac{\alpha}{C}e^{-Stos}}{S\left(S + \frac{1}{RC}\right)}\right\}$$

Again using partial fraction expansion and manipulating gives:

$$V_{SS}(t) = \left[1 - \frac{\alpha R + \beta}{e^{t_{OS/RC}}}\right]e^{-(t-t_{os})/RC} \quad t_{OS} < t < T.$$

The lowest point on the steady state wave can be found by evaluating:

$V_{SS}(t)\,|_{0<t<t_{OS}}$ @ $t = 0$ which gives $V_{LOW} = -\beta$.

Likewise the highest value of the wave can be found at t_{OS} which gives:

$V_{HIGH} = \alpha R - (\alpha R + \beta)e^{-tos/RC}$ and substituting β gives:

$$V_{HIGH} = \alpha R - \alpha R\left[1 - \frac{[1 - e^{t_{os}/RC}]}{[1 - e^{T/RC}]}\right]e^{-t_{os}/RC}.$$

Finally the p–p ripple is found by subtracting V_{LOW} from V_{HIGH}. After more manipulation Equation 3 results.